Fig.1A

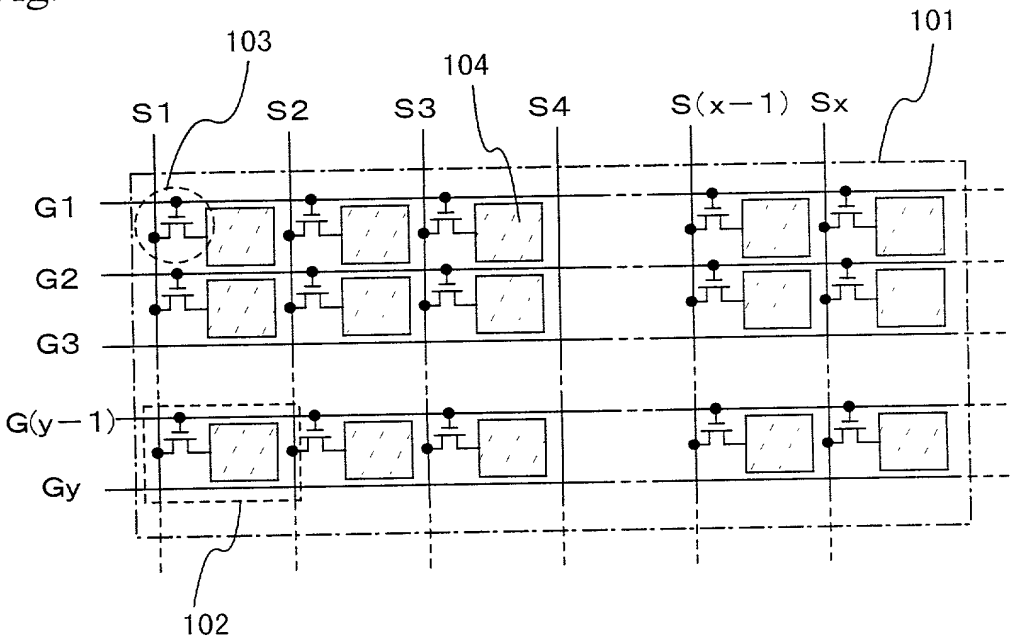


Fig.1B

(1、1)	(1、2)	(1、3)	(1、4)	(1、5)		(1、x)
(2、1)	(2、2)	(2、3)	(2、4)	(2、5)		(2、x)
(3、1)	(3、2)	(3、3)	(3、4)	(3、5)		(3、x)
(y、1)	(y、2)	(y、3)	(y、4)	(y、5)		(y、x)

Fig.2

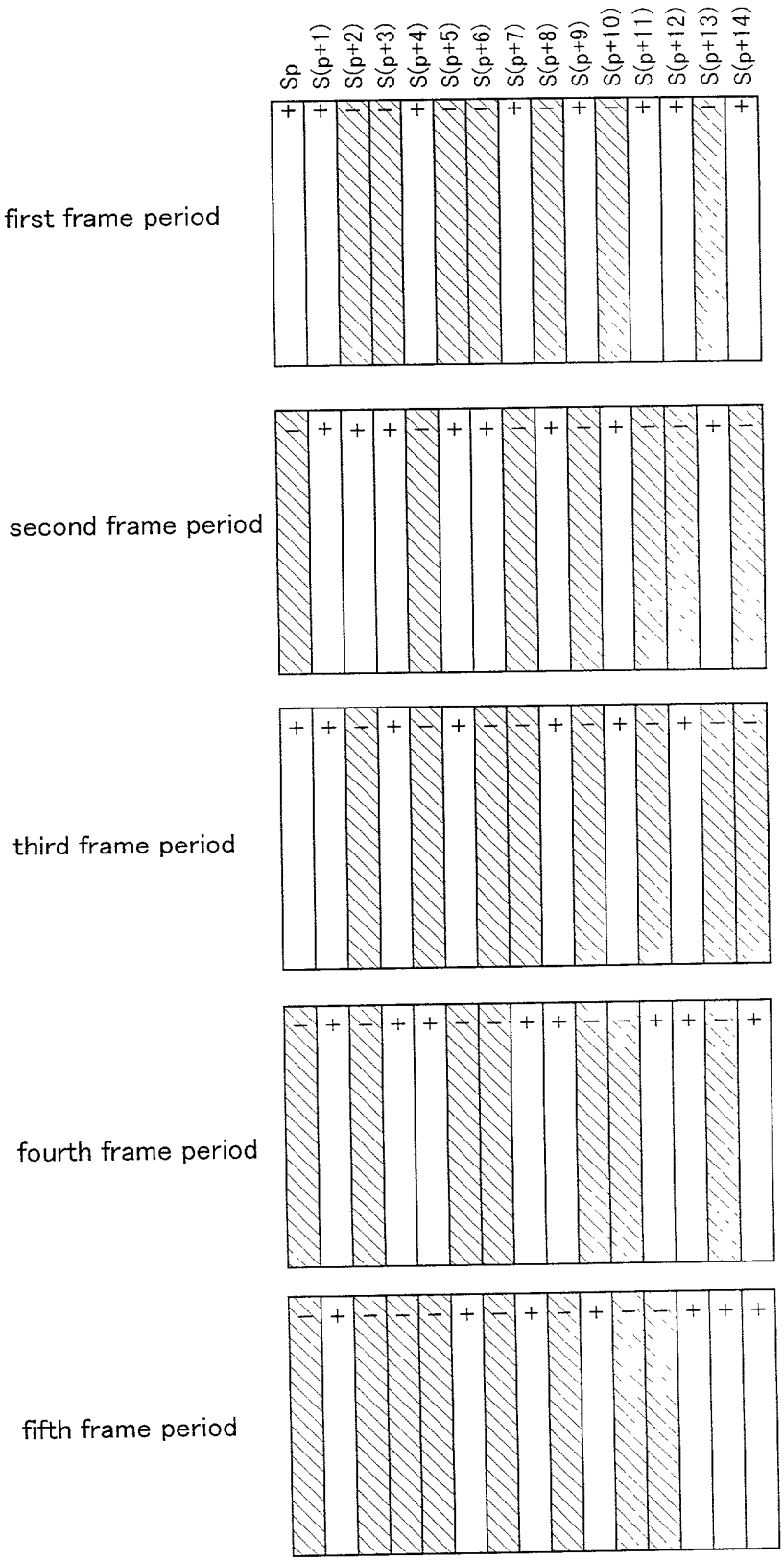

Sp
S(p+1)
S(p+2)
S(p+3)
S(p+4)
S(p+5)
S(p+6)
S(p+7)
S(p+8)
S(p+9)
S(p+10)
S(p+11)
S(p+12)
S(p+13)
S(p+14)
first frame period
second frame period
third frame period
fourth frame period
fifth frame period

Fig.3

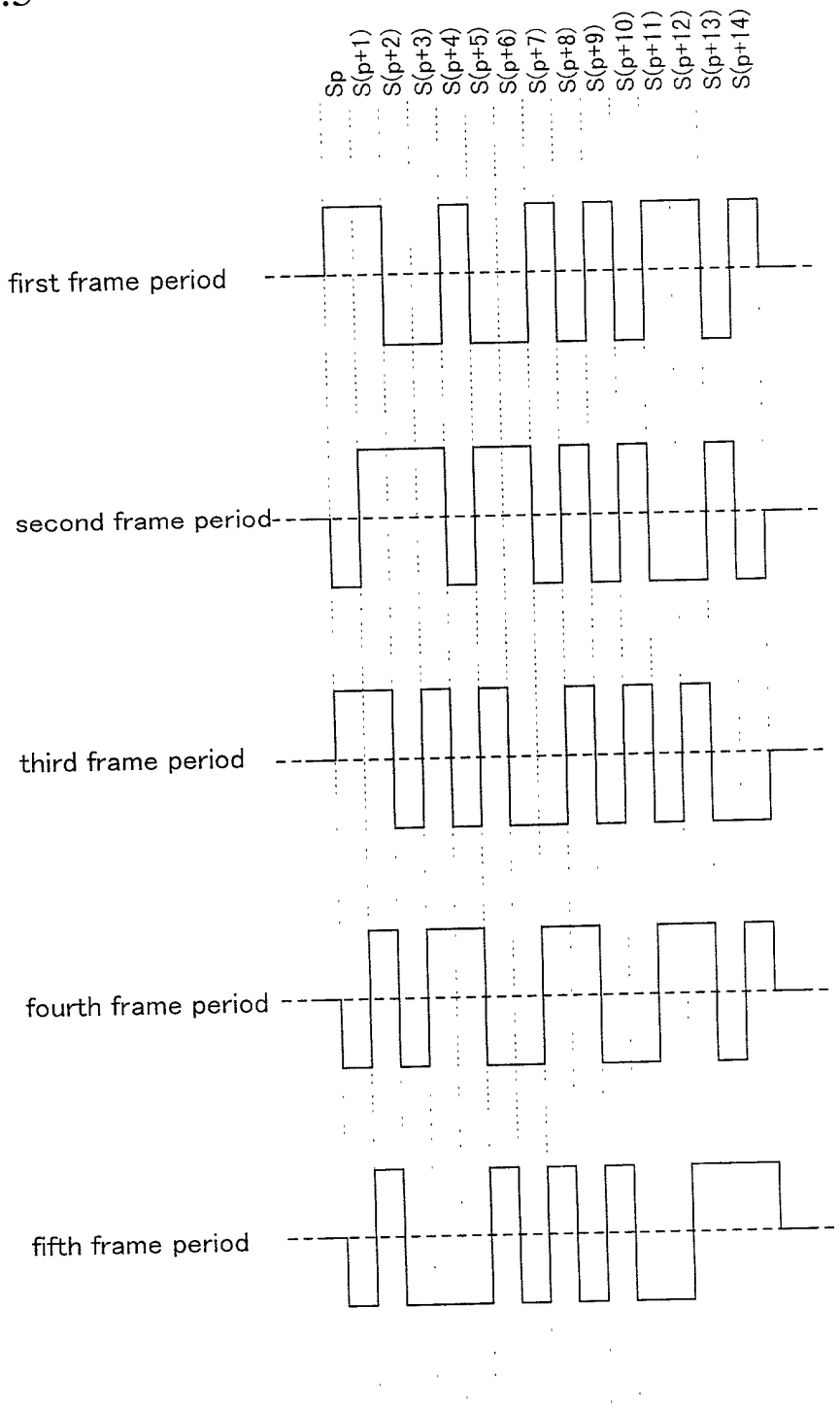

Sp
S(p+1)
S(p+2)
S(p+3)
S(p+4)
S(p+5)
S(p+6)
S(p+7)
S(p+8)
S(p+9)
S(p+10)
S(p+11)
S(p+12)
S(p+13)
S(p+14)
first frame period
second frame period
third frame period
fourth frame period
fifth frame period

Fig.4

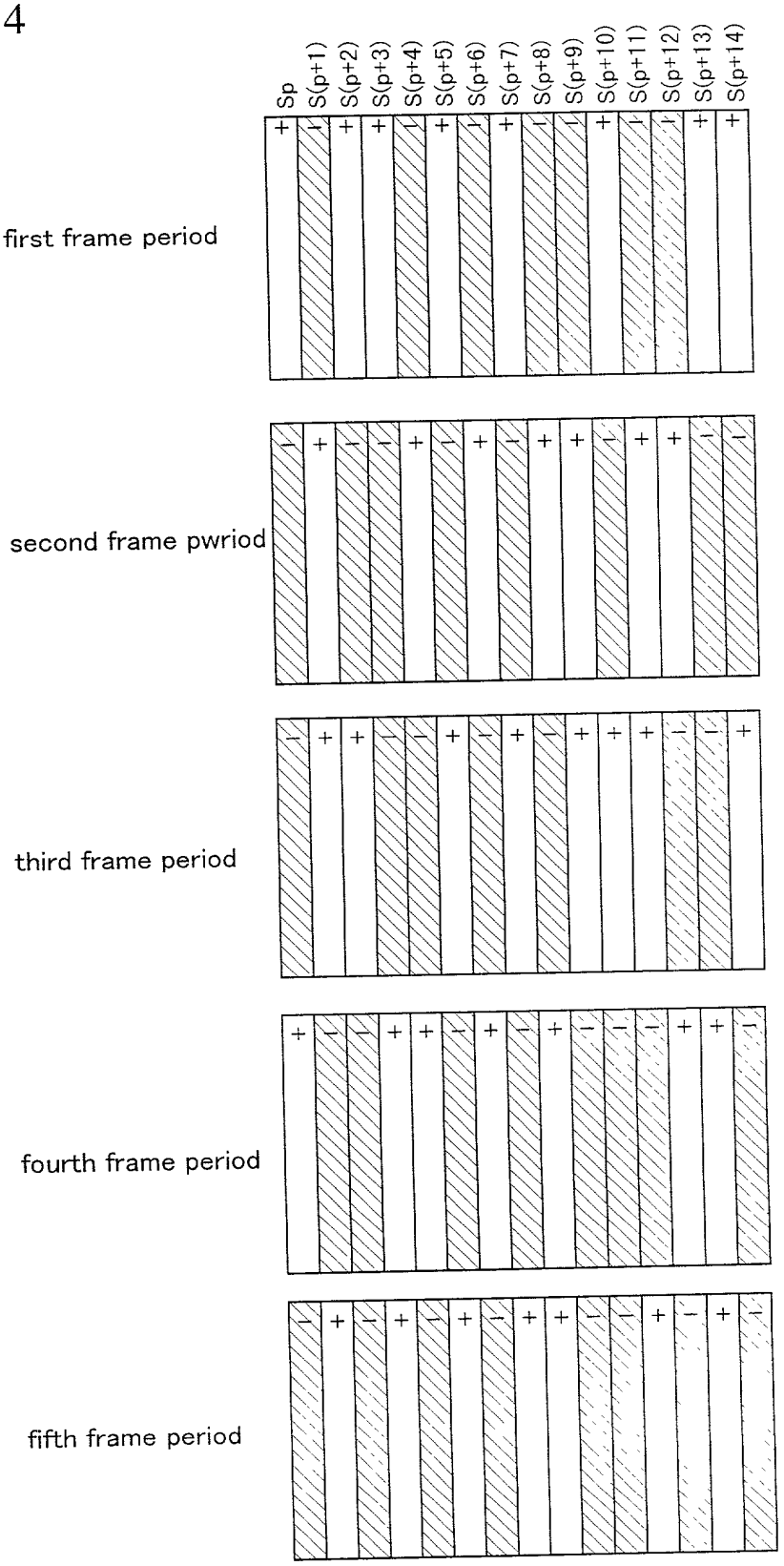

Sp
S(p+1)
S(p+2)
S(p+3)
S(p+4)
S(p+5)
S(p+6)
S(p+7)
S(p+8)
S(p+9)
S(p+10)
S(p+11)
S(p+12)
S(p+13)
S(p+14)
first frame period
second frame pwriod
third frame period
fourth frame period
fifth frame period

Fig.5

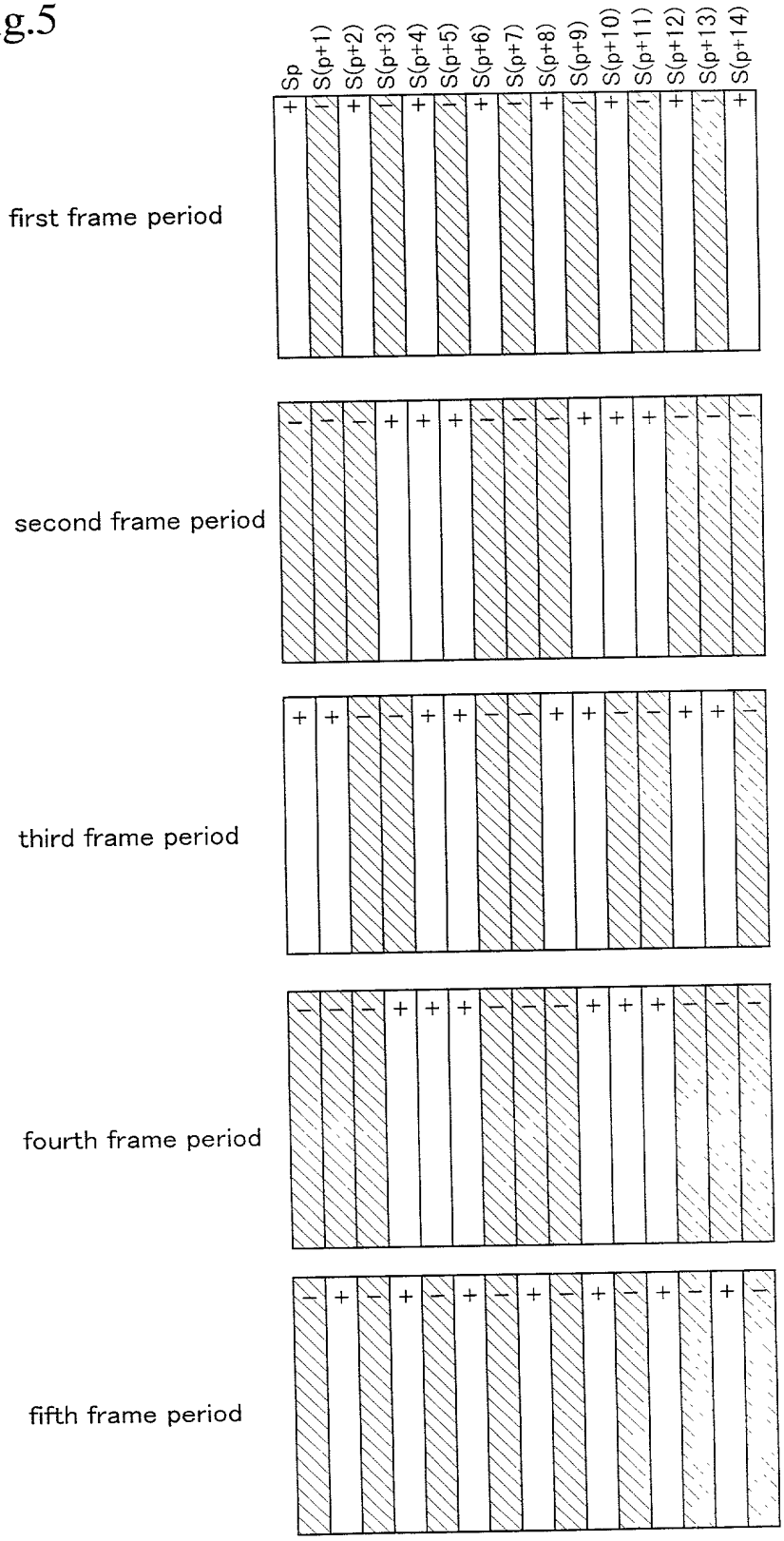

Sp
S(p+1)
S(p+2)
S(p+3)
S(p+4)
S(p+5)
S(p+6)
S(p+7)
S(p+8)
S(p+9)
S(p+10)
S(p+11)
S(p+12)
S(p+13)
S(p+14)
first frame period
second frame period
third frame period
fourth frame period
fifth frame period

Fig.6

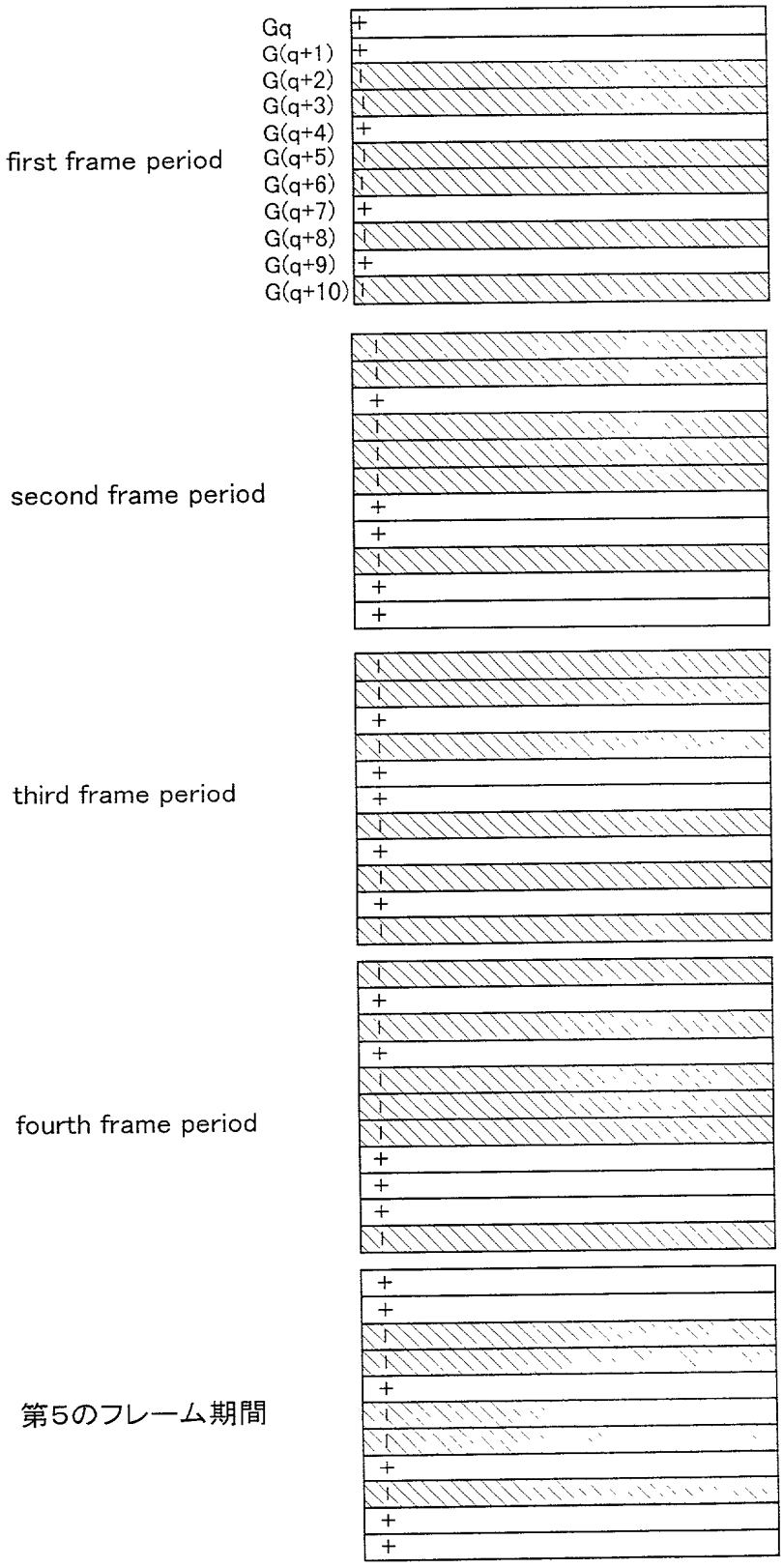

Gq
G(q+1)
G(q+2)
G(q+3)
G(q+4)
G(q+5)
G(q+6)
G(q+7)
G(q+8)
G(q+9)
G(q+10)
first frame period
second frame period
third frame period
fourth frame period
第5のフレーム期間

Fig.7

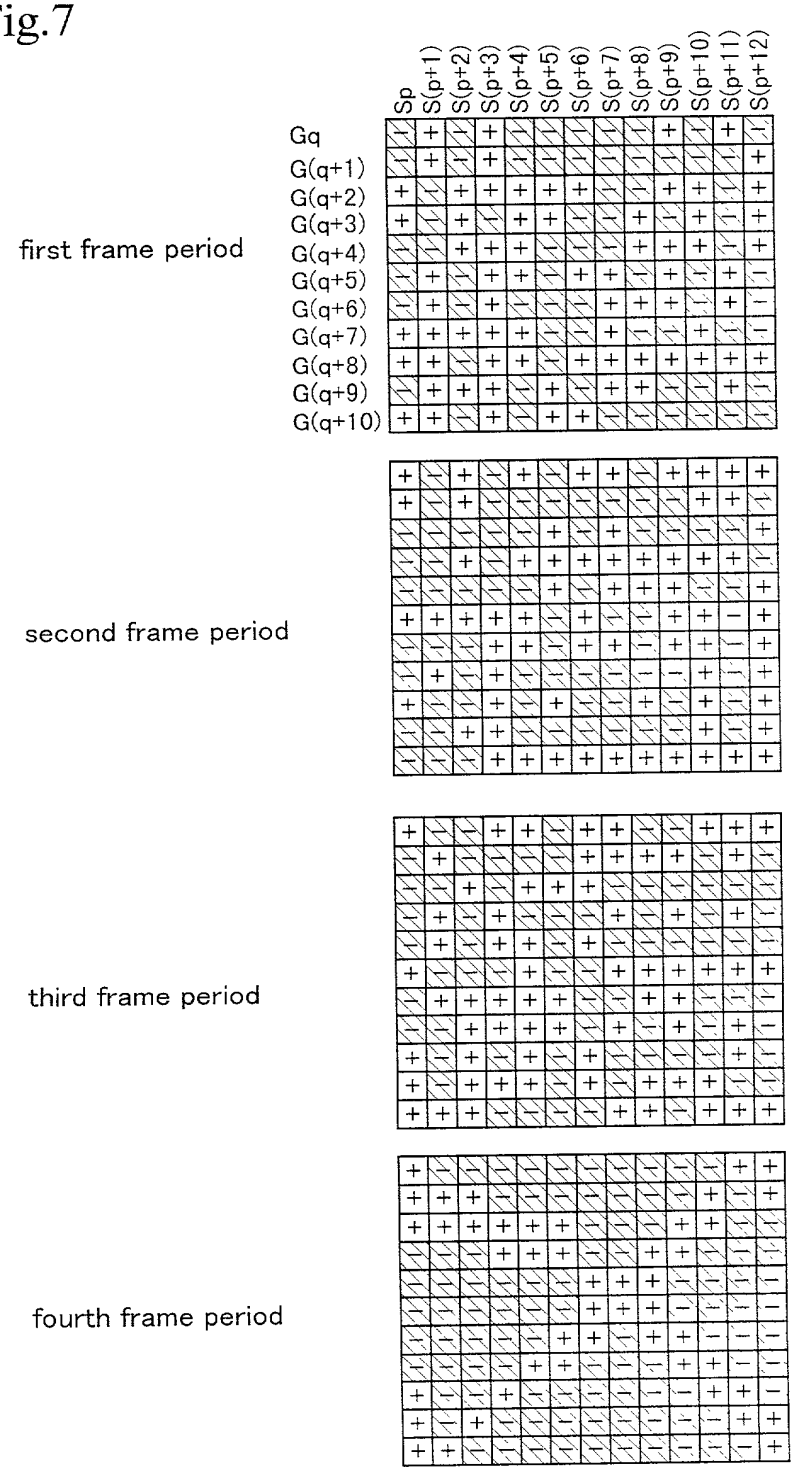

Sp
S(p+1)
S(p+2)
S(p+3)
S(p+4)
S(p+5)
S(p+6)
S(p+7)
S(p+8)
S(p+9)
S(p+10)
S(p+11)
S(p+12)
Gq
G(q+1)
G(q+2)
G(q+3)
G(q+4)
G(q+5)
G(q+6)
G(q+7)
G(q+8)
G(q+9)
G(q+10)
first frame period
second frame period
third frame period
fourth frame period

Fig.8

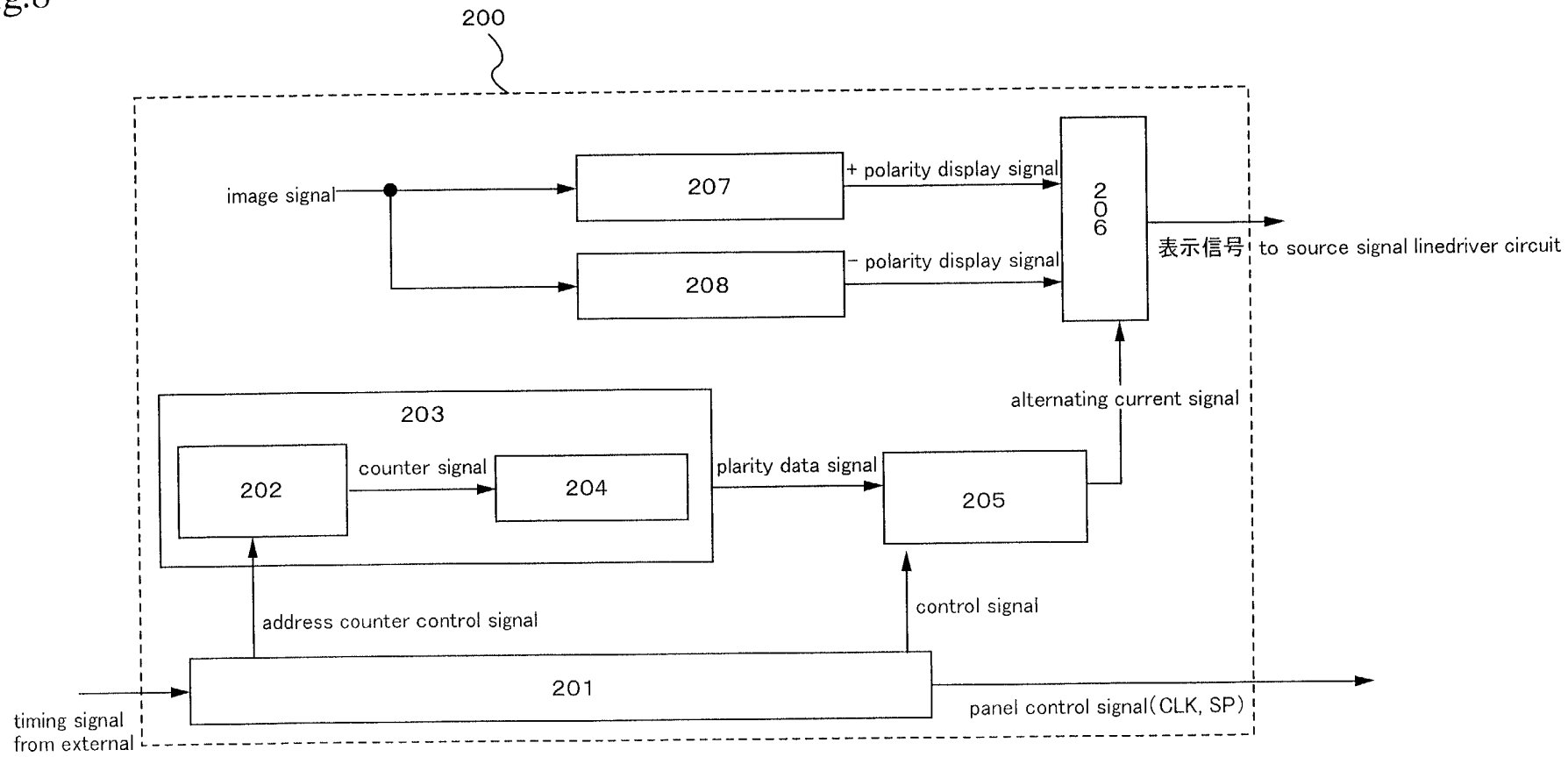
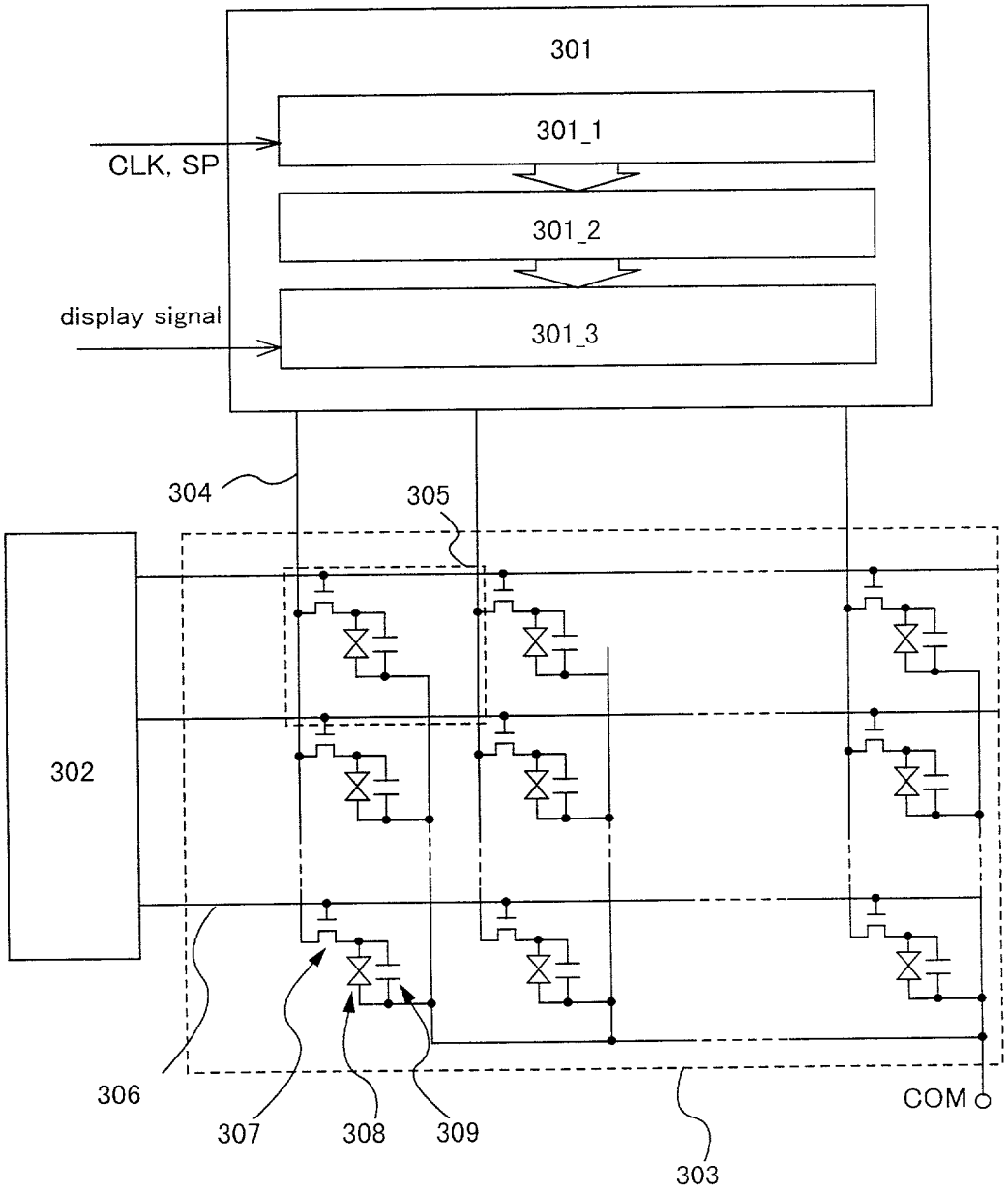

200
image signal
207
+ polarity display signal
208
- polarity display signal
206
表示信号
to source signal linedriver circuit
alternating current signal
203
202
counter signal
204
plarity data signal
205
address counter control signal
control signal
201
timing signal
from external
panel control signal(CLK, SP)

Fig.9


301
301_1
301_2
301_3
CLK, SP
display signal
304
305
302
306
307
308
309
303
COM

T08020" T9787760

Fig. 10

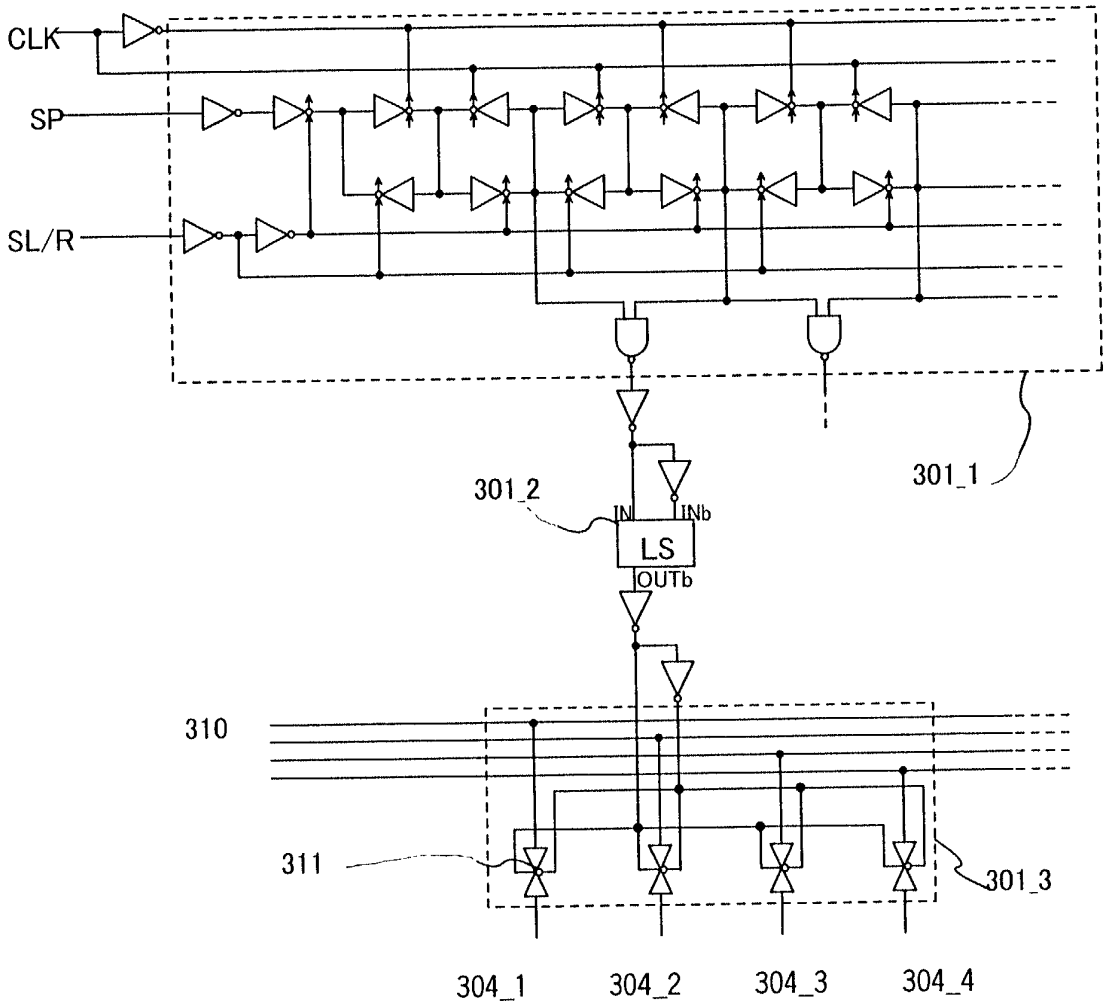


Fig.11A

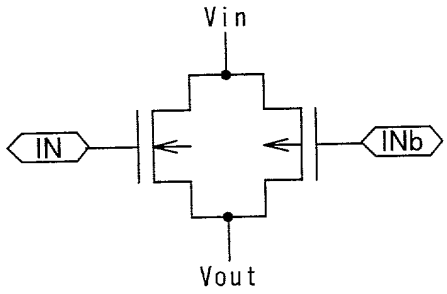


Fig.11B

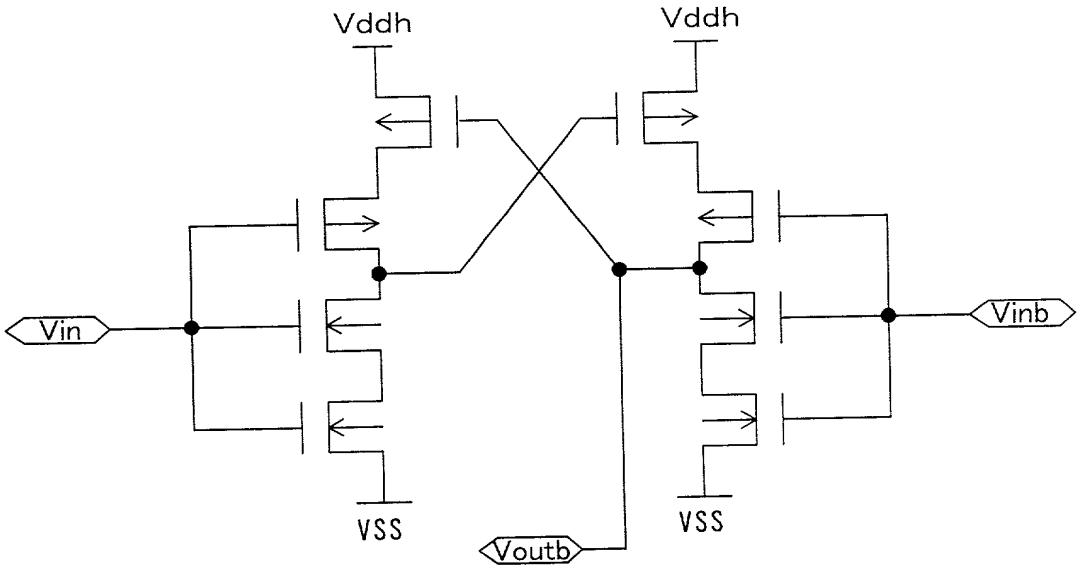
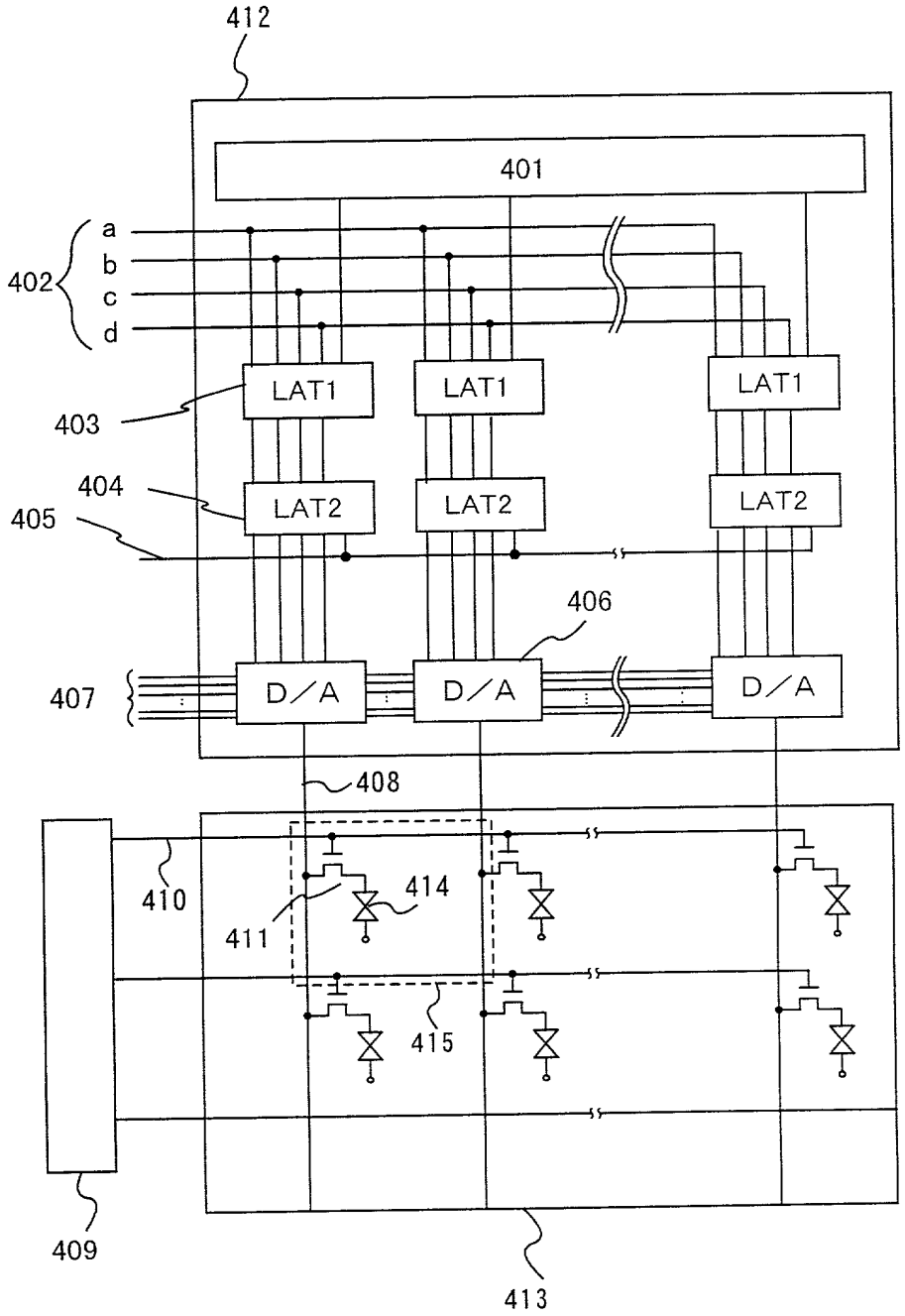


Fig.12


412
401
a
b
c
d
402
LAT1
LAT1
LAT1
403
404
LAT2
LAT2
LAT2
405
406
407
D/A
D/A
D/A
408
410
411
414
415
409
413

T08020 T97827609

Fig.13A

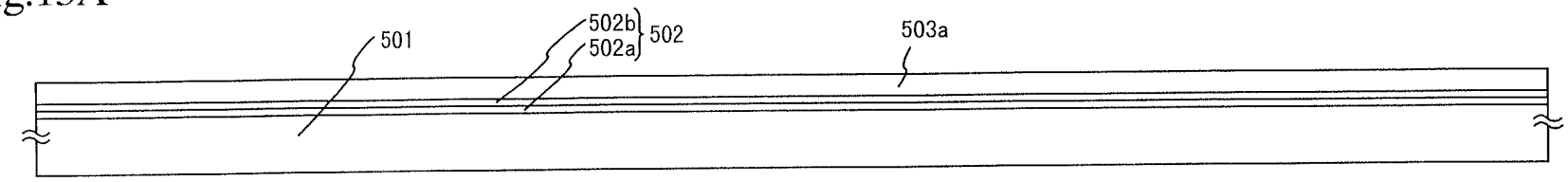


Fig.13B

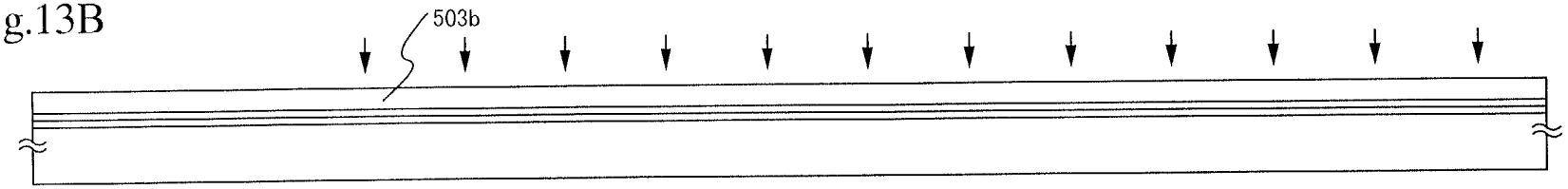


Fig.13C

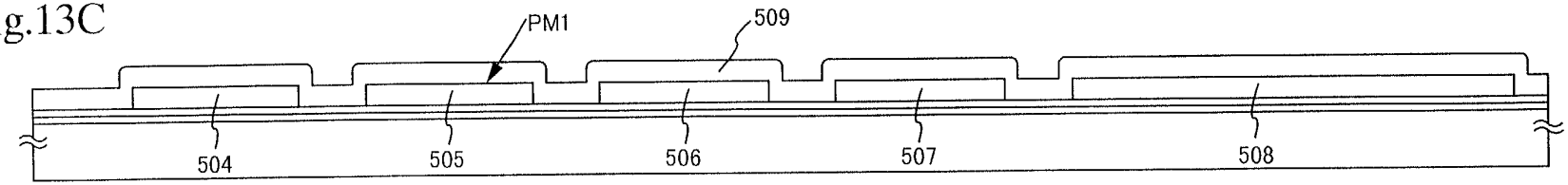


Fig.13D

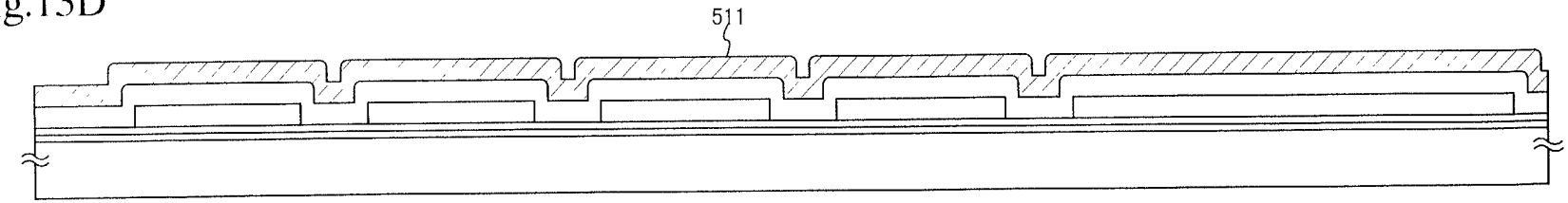


Fig.14A

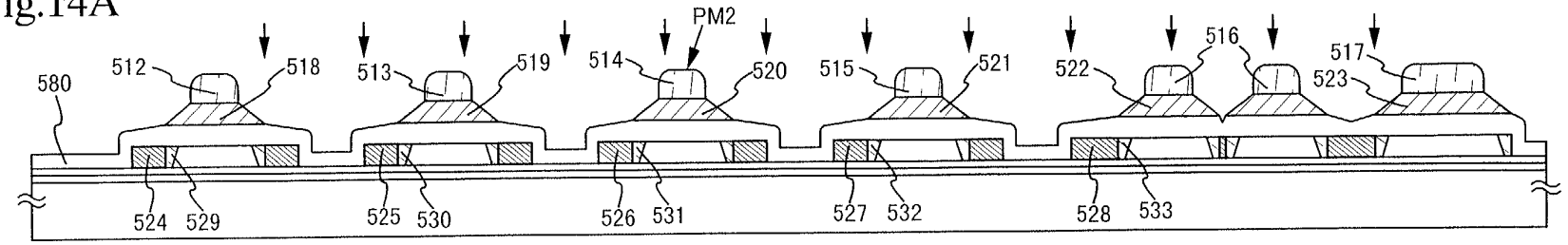


Fig.14B

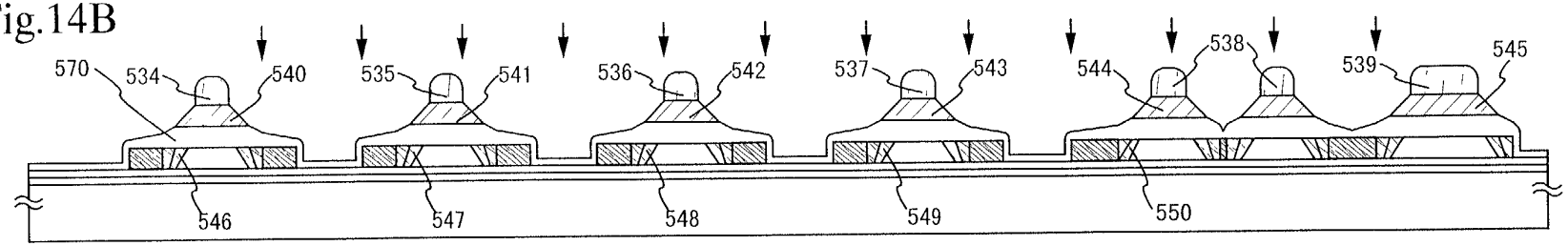


Fig.14C

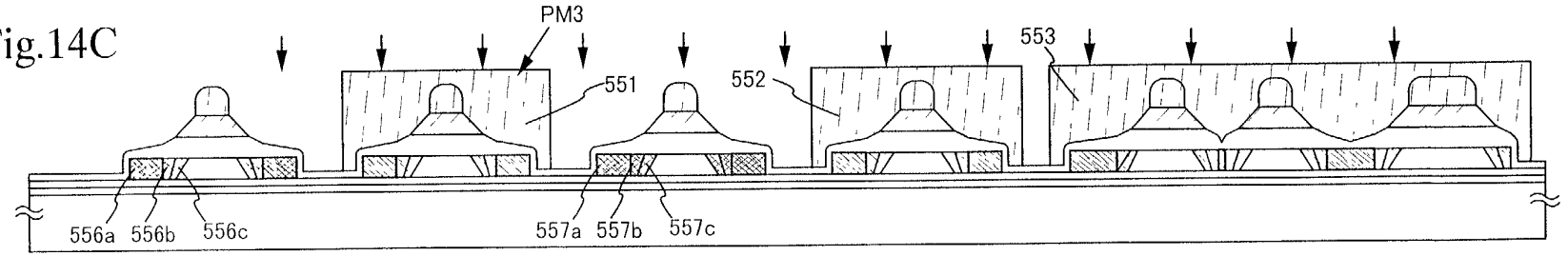


Fig.15A

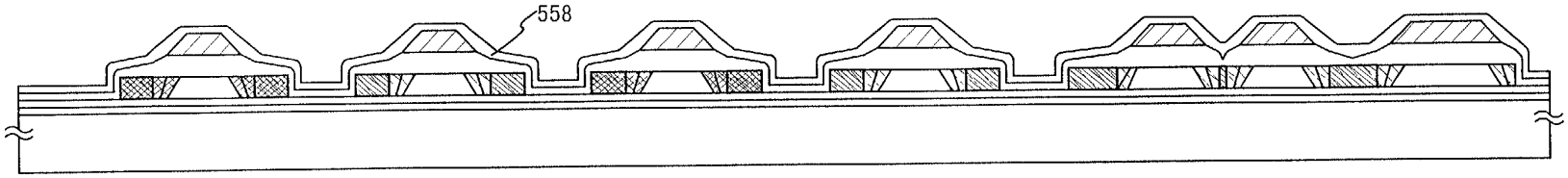


Fig.15B

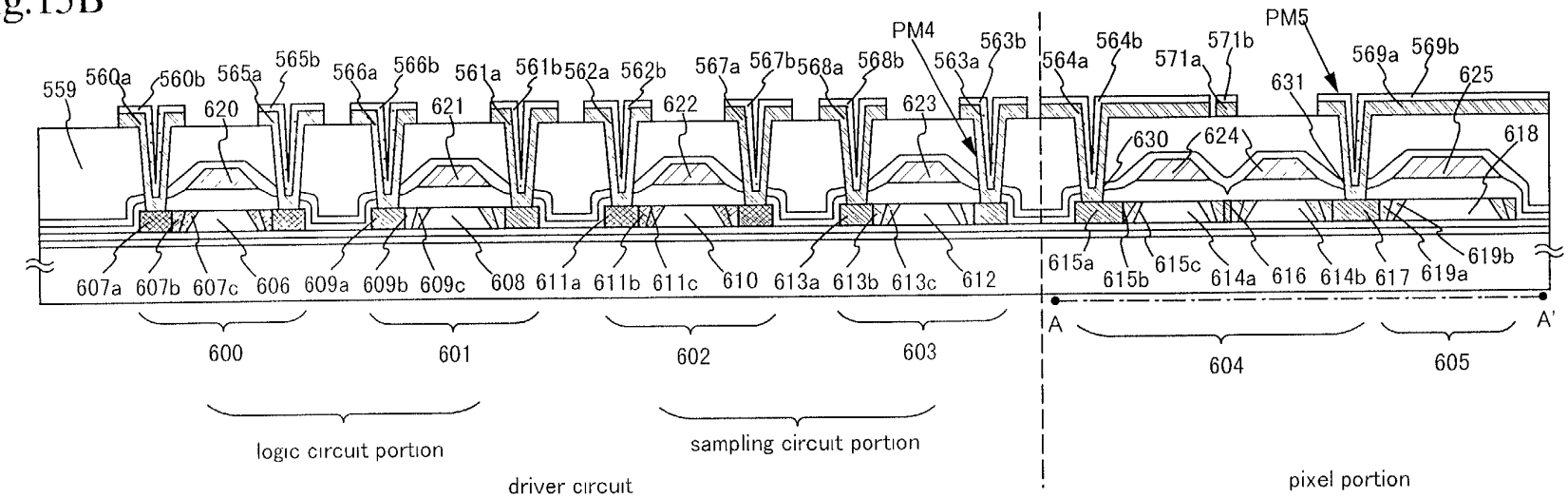
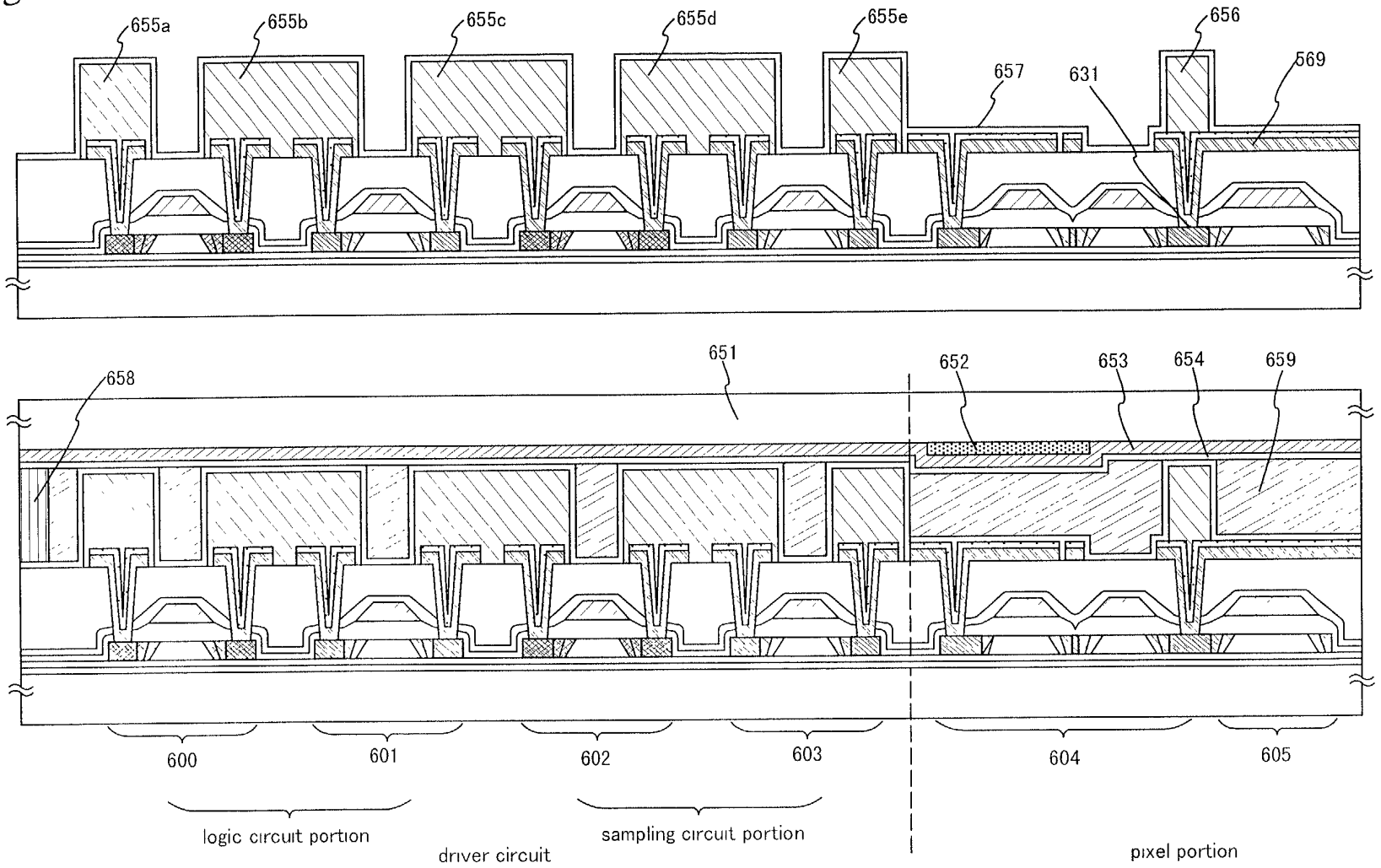


Fig.16


655a
655b
655c
655d
655e
656
657
631
569
658
651
652
653
654
659
600
601
602
603
604
605
logic circuit portion
driver circuit
sampling circuit portion
pixel portion

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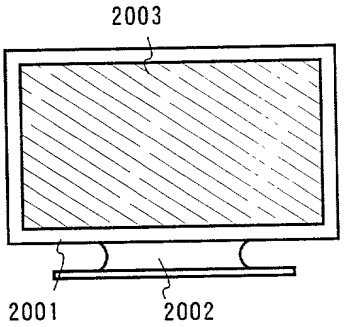


Fig.17A

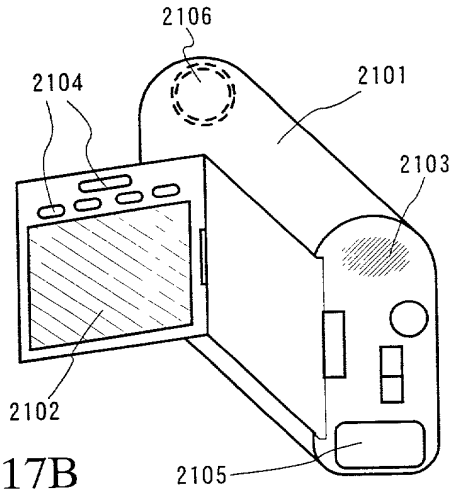


Fig.17B

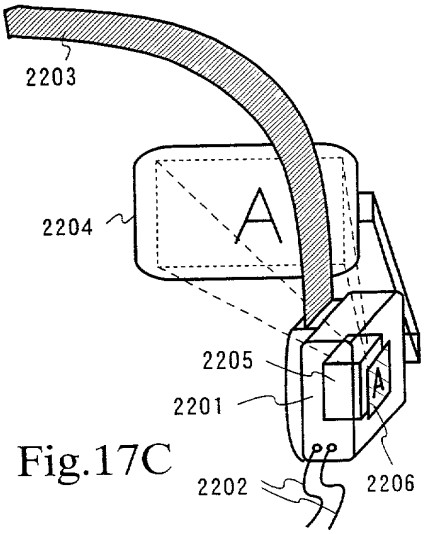


Fig.17C

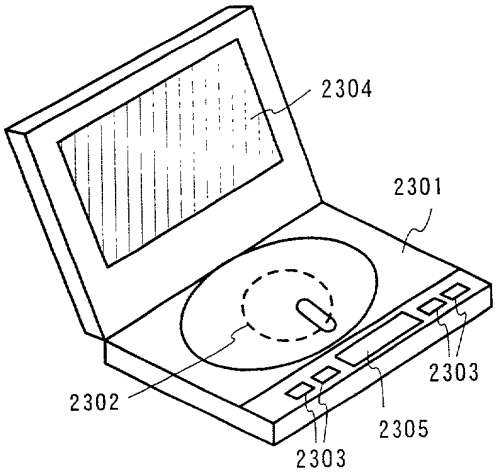


Fig.17D

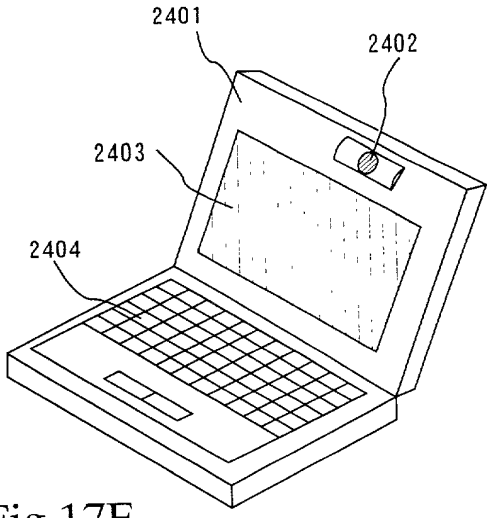


Fig.17E

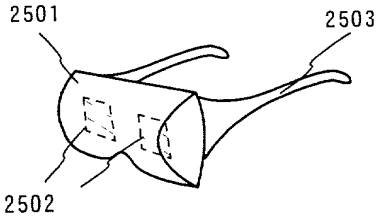


Fig.17F

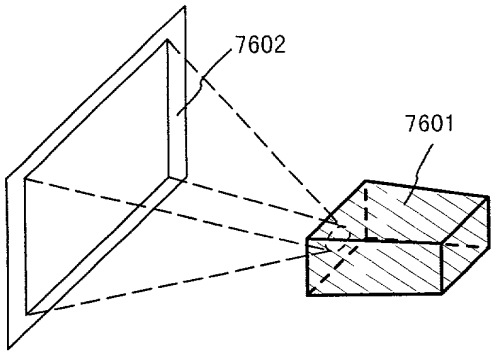


Fig.18A

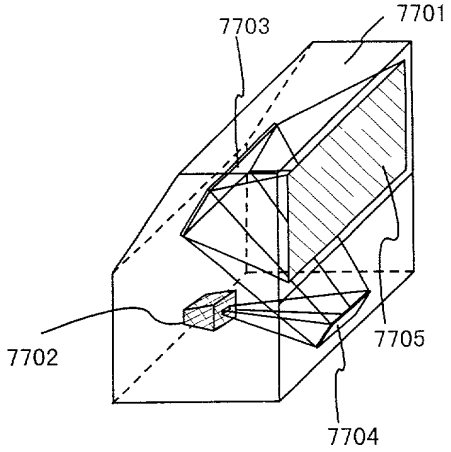


Fig.18B

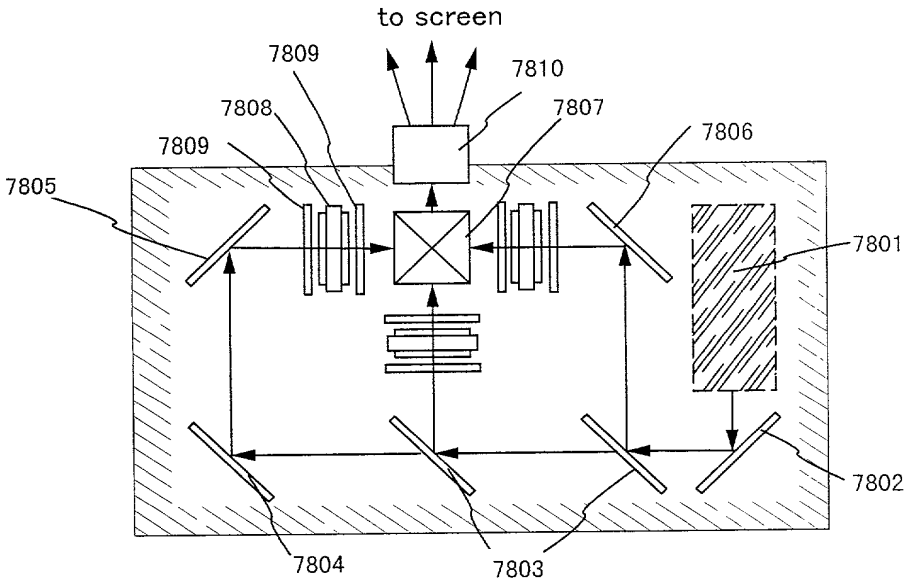


Fig.18C

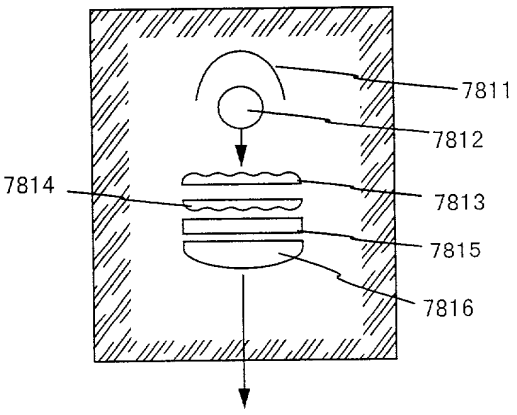


Fig.18D

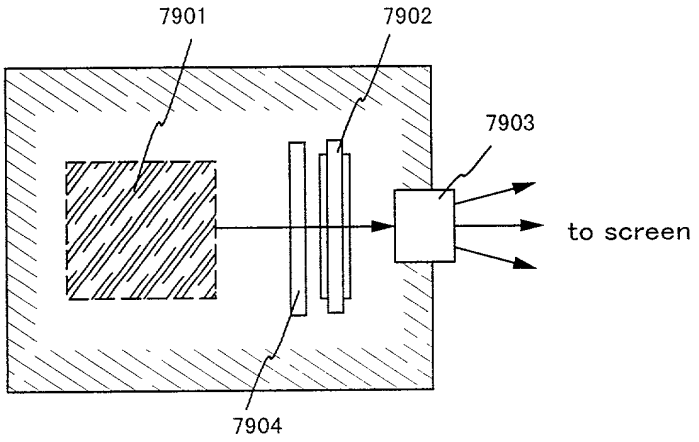


Fig.19A

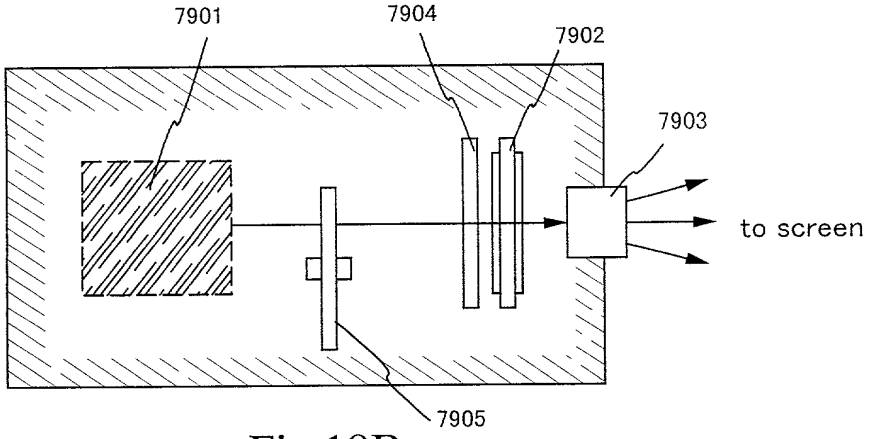


Fig.19B

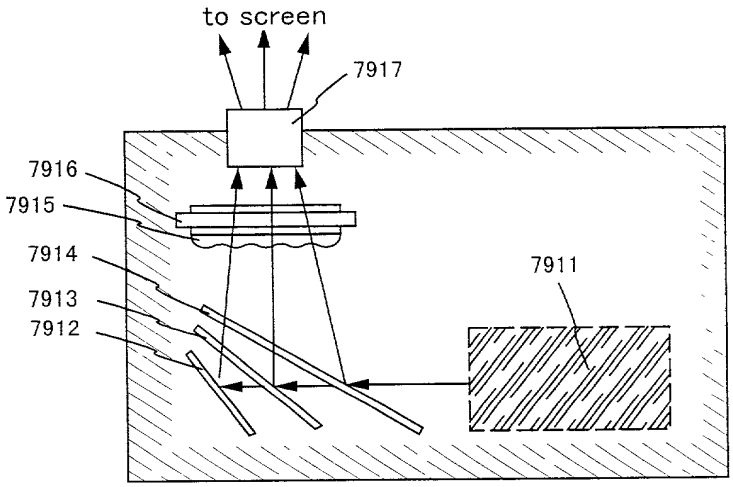


Fig.19C

Fig.20A

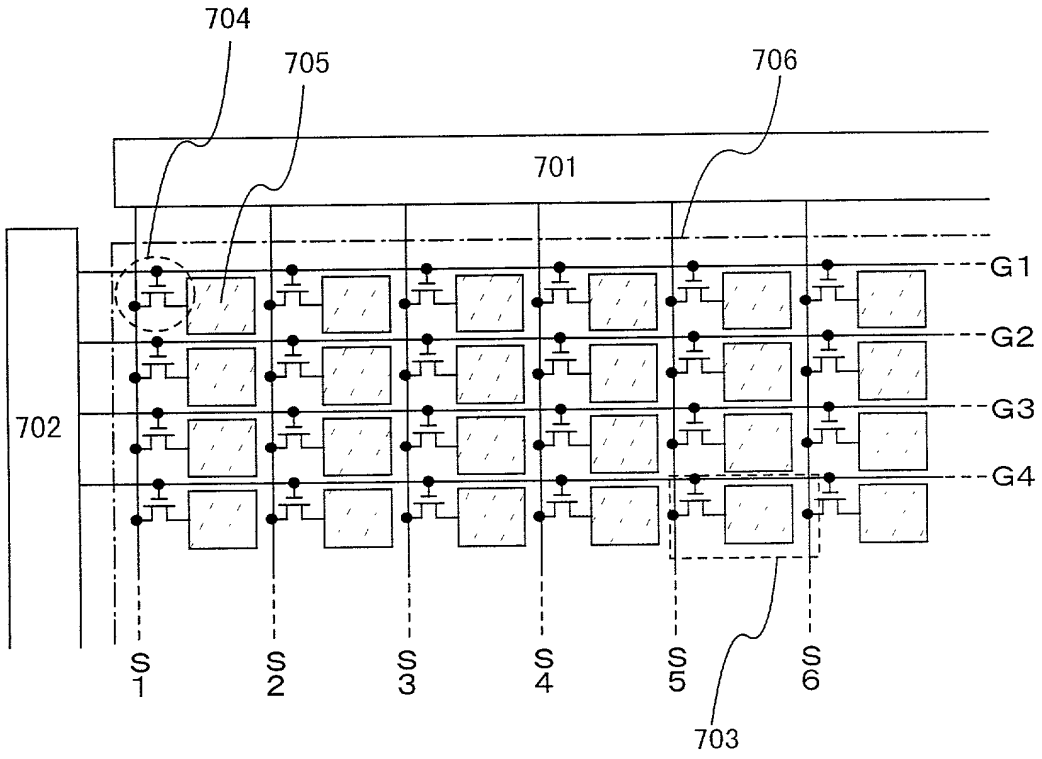
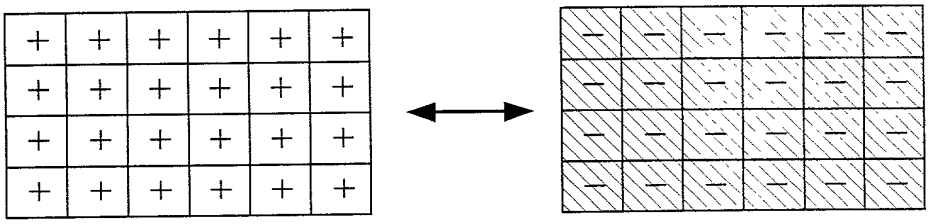


Fig.20B

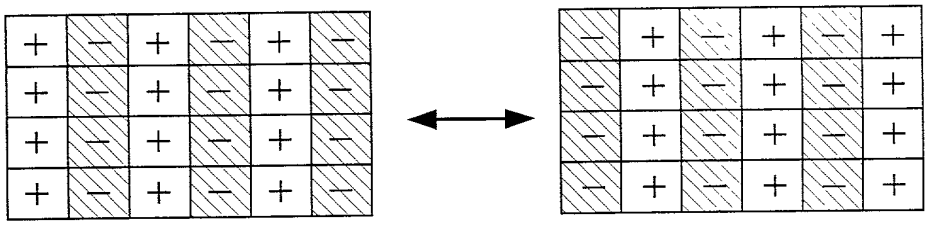
(1、1)	(1、2)	(1、3)	(1、4)	(1、5)	(1、6)
(2、1)	(2、2)	(2、3)	(2、4)	(2、5)	(2、6)
(3、1)	(3、2)	(3、3)	(3、4)	(3、5)	(3、6)
(4、1)	(4、2)	(4、3)	(4、4)	(4、5)	(4、6)

Fig.21A



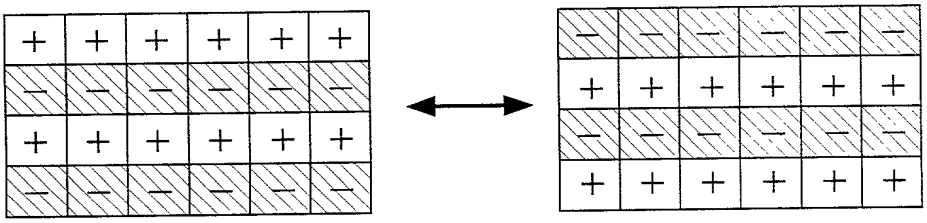
polarity pattern 1　　polarity pattern 2

Fig.21B



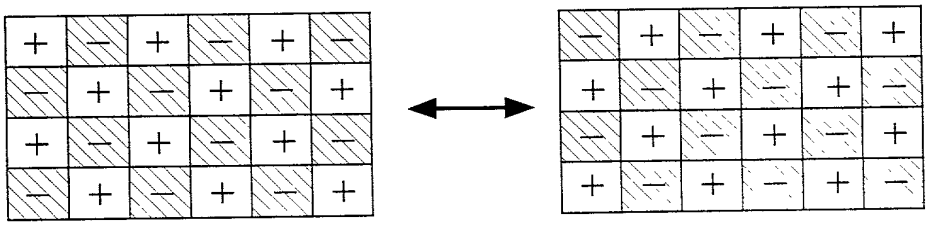
polarity pattern 3　　polarity pattern 4

Fig.21C



polarity pattern 5　　polarity pattern 6

Fig.21D



polarity pattern 7　　polarity pattern 8

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Fig.22

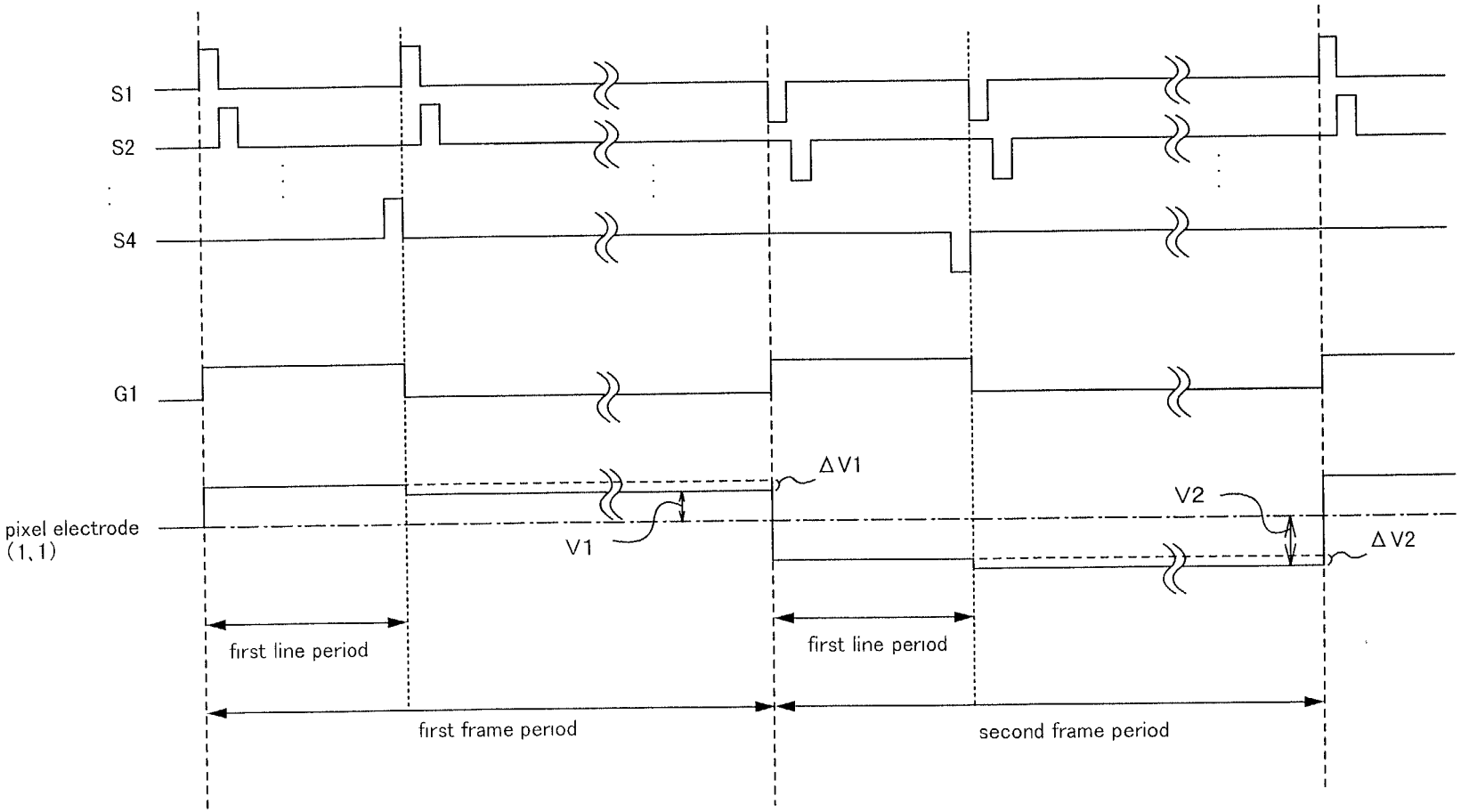
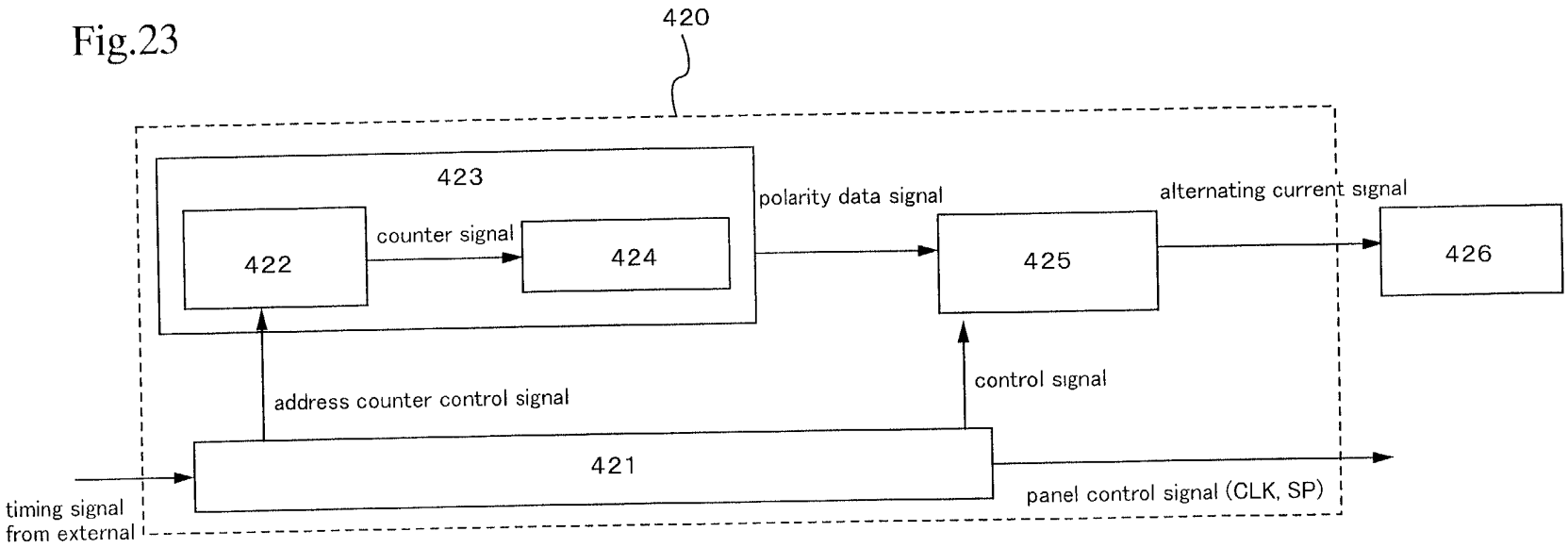

S1
S2
S4
G1
pixel electrode
(1,1)
ΔV1
V1
V2
ΔV2
first line period
first line period
first frame period
second frame period

Fig.23


420
423
422
counter signal
424
polarity data signal
425
alternating current signal
426
address counter control signal
control signal
421
timing signal
from external
panel control signal (CLK, SP)